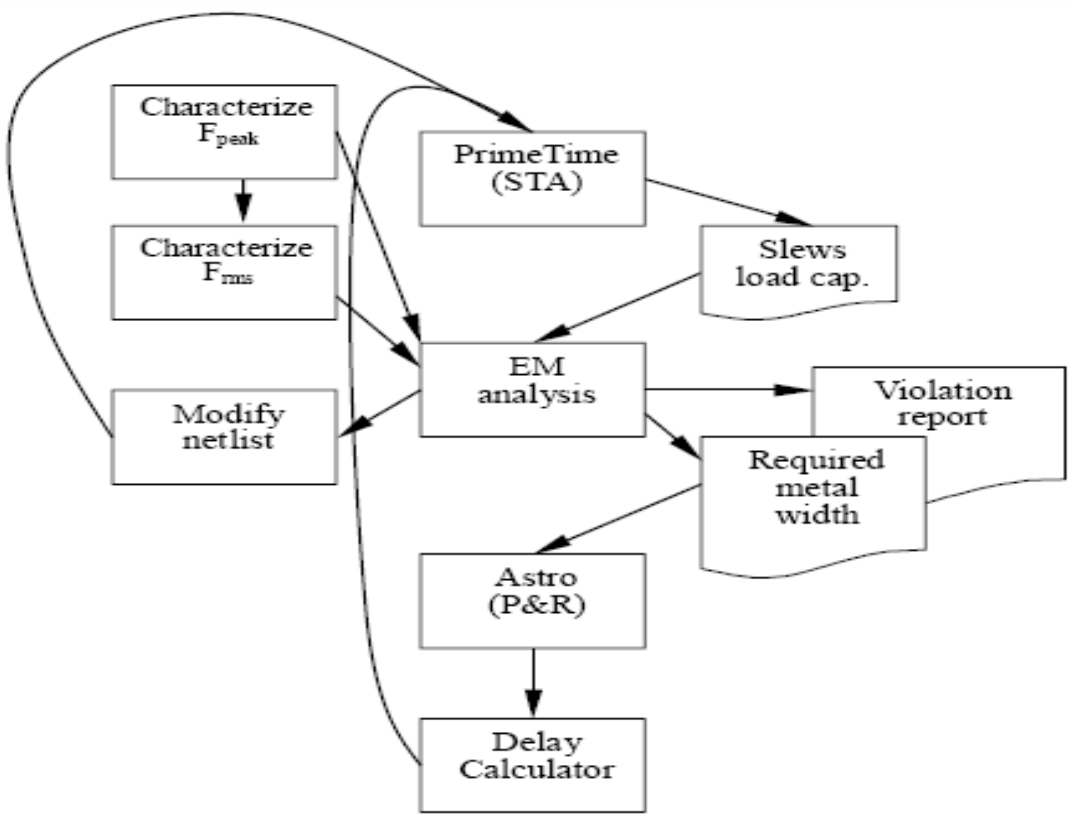
65nm Signoff

Contents

- Signal EM Flow
- Power Grid Sign-off
- Timing Closure & Sign-off
- Dummy filling flow & Timing fixing
- Others

Signal EM Analysis

- Peak/Avg./RMS current
- AstroRail or TSMC utility (Ref. Flow 4.0/5.0)



Signal EM Analysis Procedure

1. The temperature for the signal EM analysis: 125C.
2. The RC corner for the RC extraction: Cworst in 125C.
3. The power consumption is calculated in the LT corner, or the ML corner.
4. Set the reasonable switching activity in the signal EM analysis.

Power Integrity

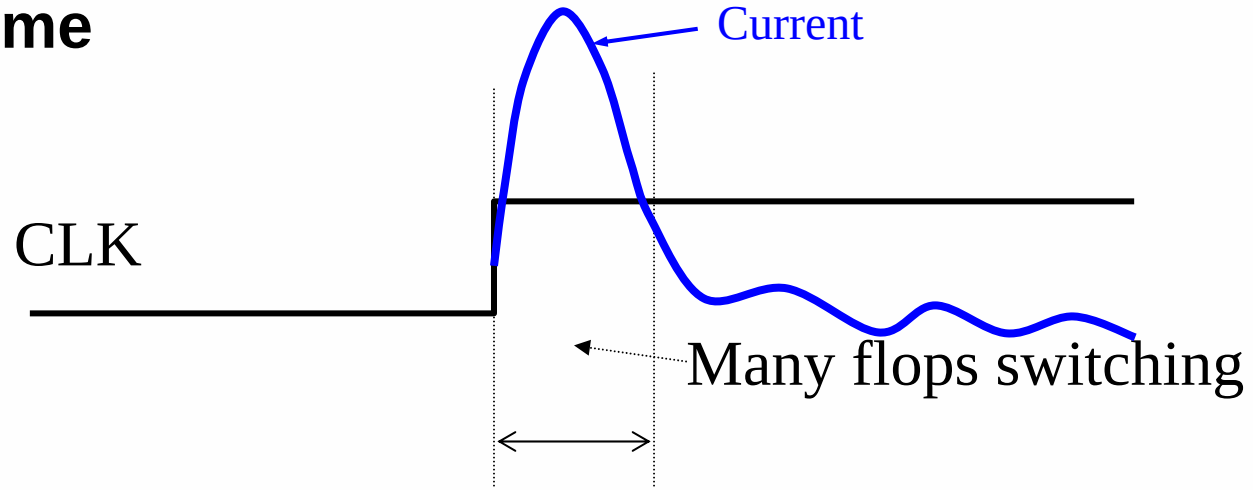
- Power grid signed-off in three modes
  - Static IR drop
    - Average power IR drop < 5% VDD+VSS (wire-bond) 3% (Flip chip)
  - Dynamic IR drop
    - 4-5X Static IR < 15% VDD + VSS
    - Dcap insertion
  - Scan Peak IR around clock-edge < 30% VDD
    - Peak power usually around clock-edge
    - Seen many chips failing even in scan-mode
    - Analyzing IR drop during small timing window when flops are switching
- Power reductions
  - Leakage: Multi-Vt by default
  - Dynamic: RTL clock gating is highly recommended
  - Comprehensive power approaches for portable device

Power Integrity Procedure

1. The temperature for the power EM analysis: 125C.
2. The RC corner for the RC extraction: CWorst in 125C.
3. The power consumption is calculated in the LT corner, -40C/110% VDD/FF, or the ML corner.
4. Set the reasonable toggle rate to calculate the average power consumption.
5. The EM spec is tight in 125C, the current is large in the LT or ML corner, and the power EM criterion in such condition should be most robust.

Scan Peak Power

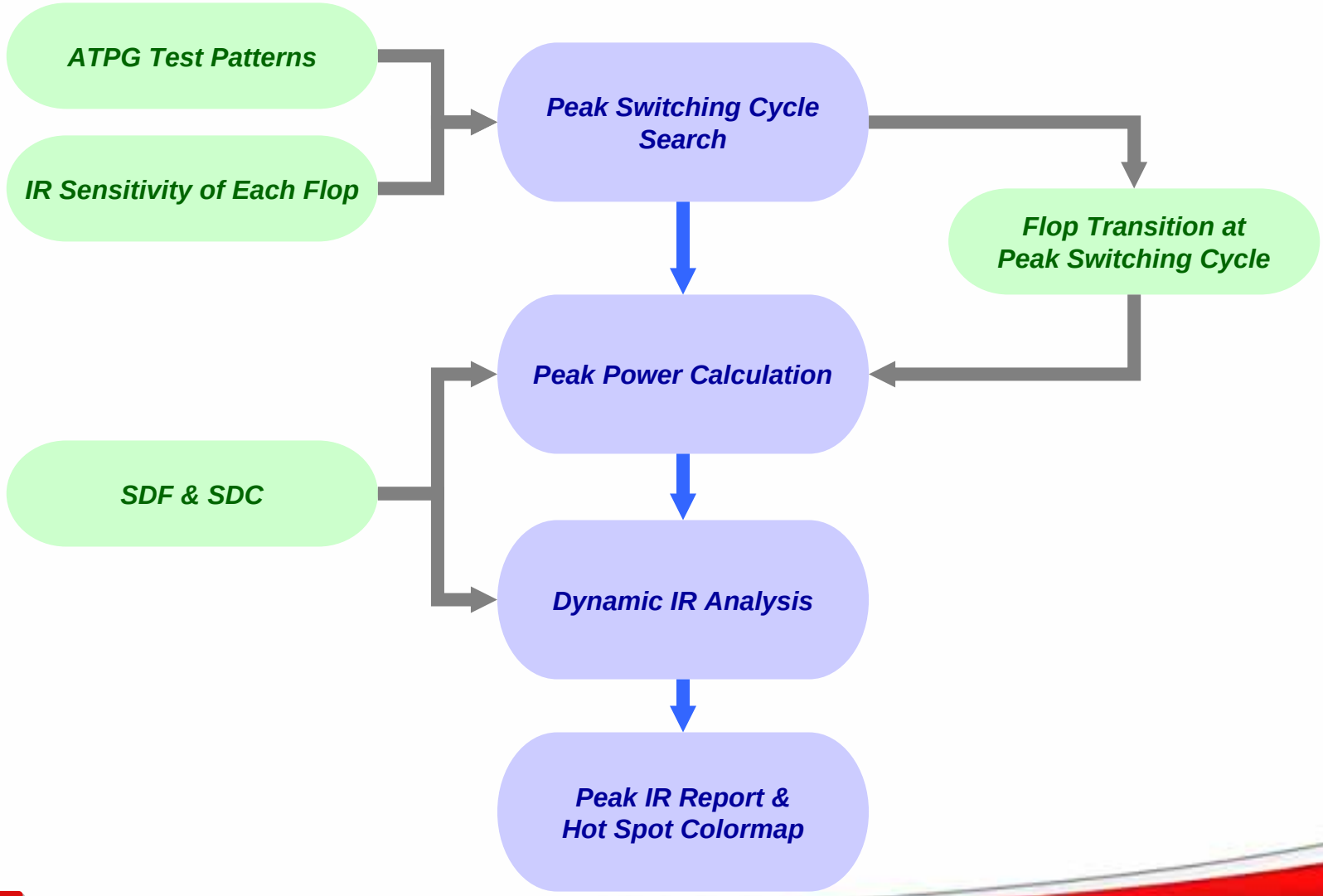
- **The most of flops are switching at almost the same time**



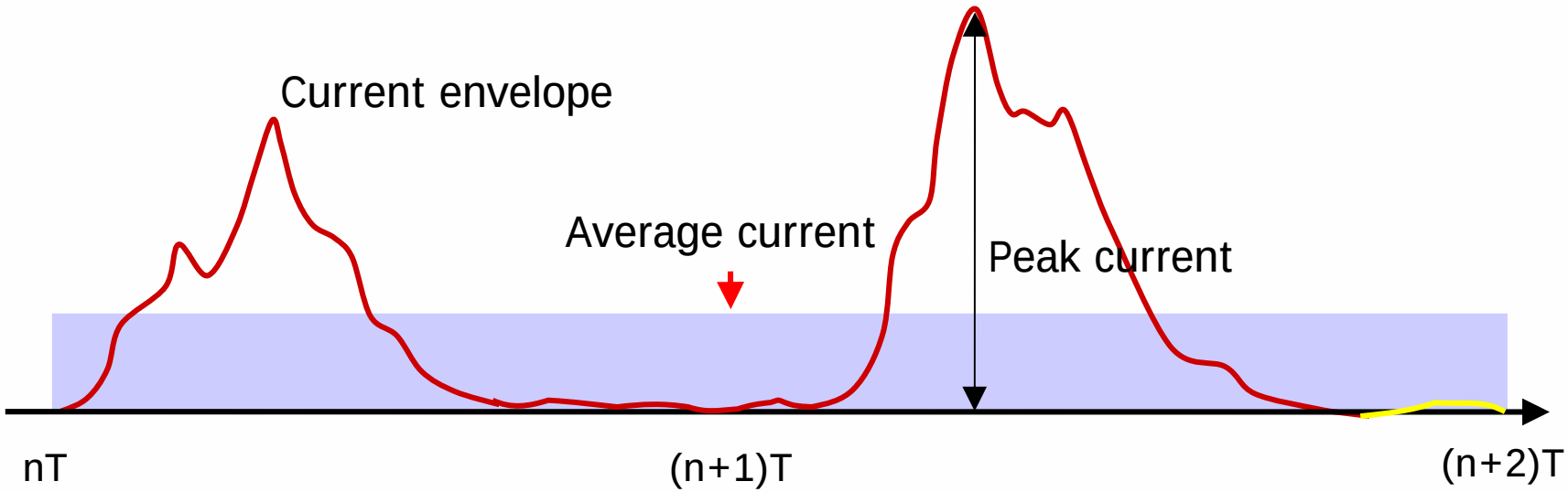
Timing window (t)

Clock skew + Average CK-Q delay + Average Transition/2

Scan Power Analysis



Static vs. Dynamic IR-drop



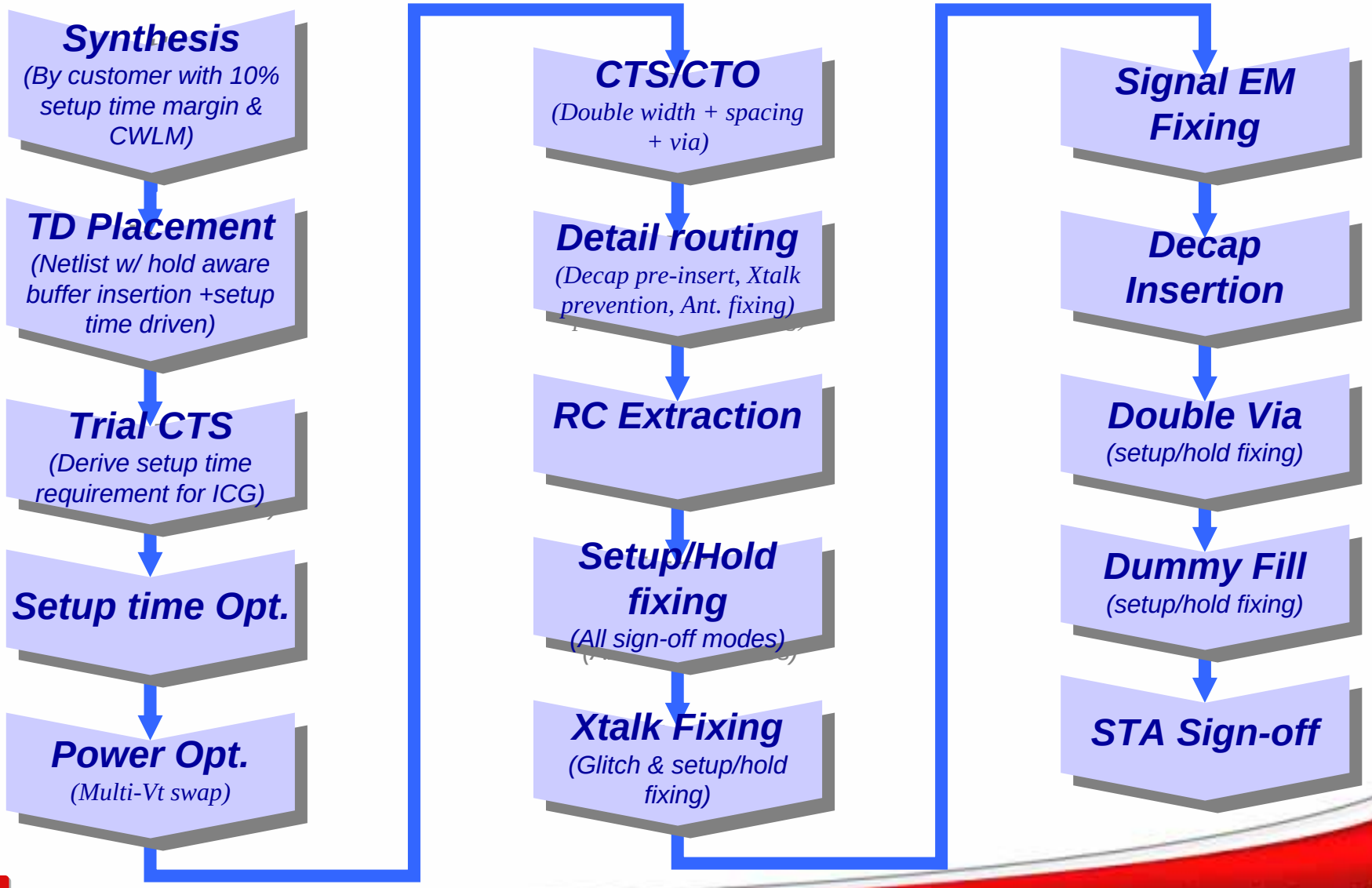
- Wire sizing can be used to control static IR-drop
- Critical de-cap provides immediate spike filtering

65nm PI sign off criteria

Technology node: 65nm			PI sign off criteria recommended				
			Package				Corner
			Wirebond		Flipchip		
			w/o pkg	w/ pkg	w/o pkg	w/ pkg	
Static			5%	5%	3%	3%	FF/SS VDD: TT
Dynamic	Function	VCD	10%	15-18%	8-10%	13-15%	FF/SS VDD: TT
		Vectorless	10%	15-18%	8-10%	13-15%	FF/SS VDD: TT
	Scan	VCD	10%	15-18%	8-10%	13-15%	FF, TT VDD: TT
		Vectorless	10%	15-18%	15-18%	13-15%	FF, TT VDD: TT

IR limit : VDD+GND

Timing Closure

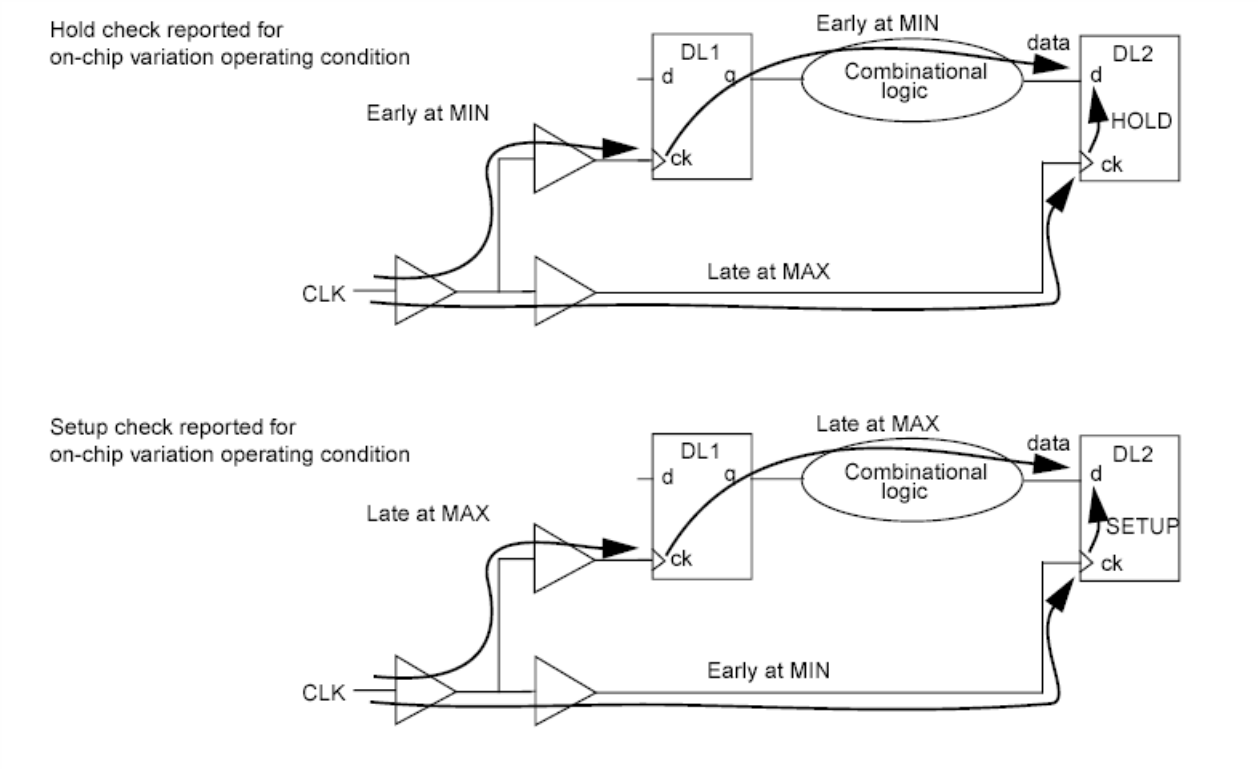


Timing Sign-off

- Timing closure taking all kinds of following effects into account
  - Multi-mode STA
  - Multiple Device & RC Corners
    - WC, WCL, BC or LT (-40C)
    - Cworst, Cbest (RCworst, RCbest, RCtypical)
  - OCV, Hold margin
  - Crosstalk
  - DFM – Dummy metals, Dummy Vias

OCV

- **OCV – On Chip Variation**



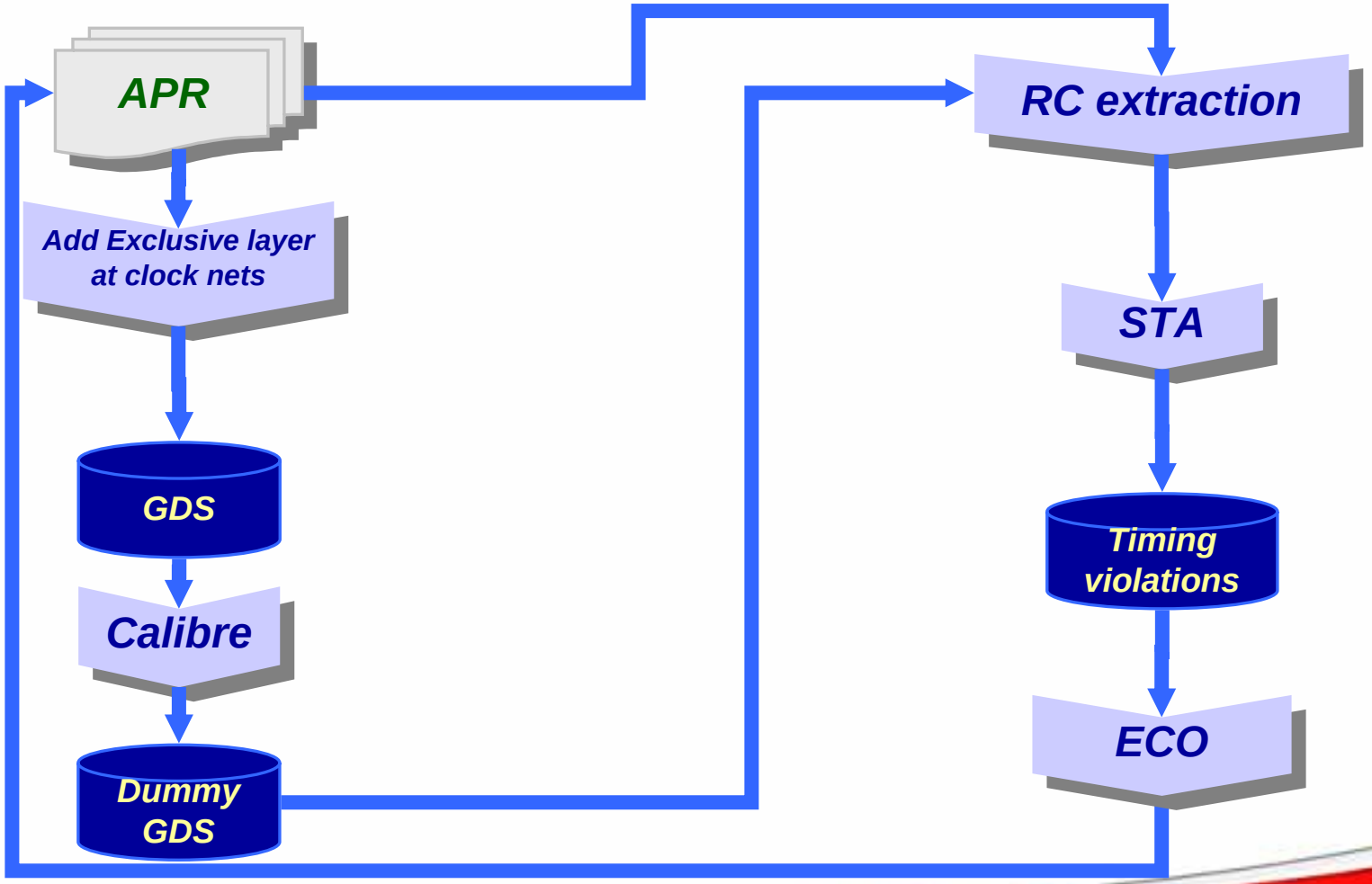
Timing Sign-off Recommendation

- Clock jitter is not included

	WC + Cworst	WCL + Cworst	BC or LT + Cbest/Cworst	Max. transition	OCV	Setup margin	Hold margin
65nm	Setup/ hold	Setup/ hold	hold	0.6ns*	WC: 5% BC:10%	0	50ps

*Max transition applied at WC corner.
*Over constraint is recommended at APR stage.
**Typical number showed here:
- OCV and Hold margin design dependant: transition, cell types, IR-drop
**Corner shown here:
- It is the basis. Customer should add more corners based on product application.

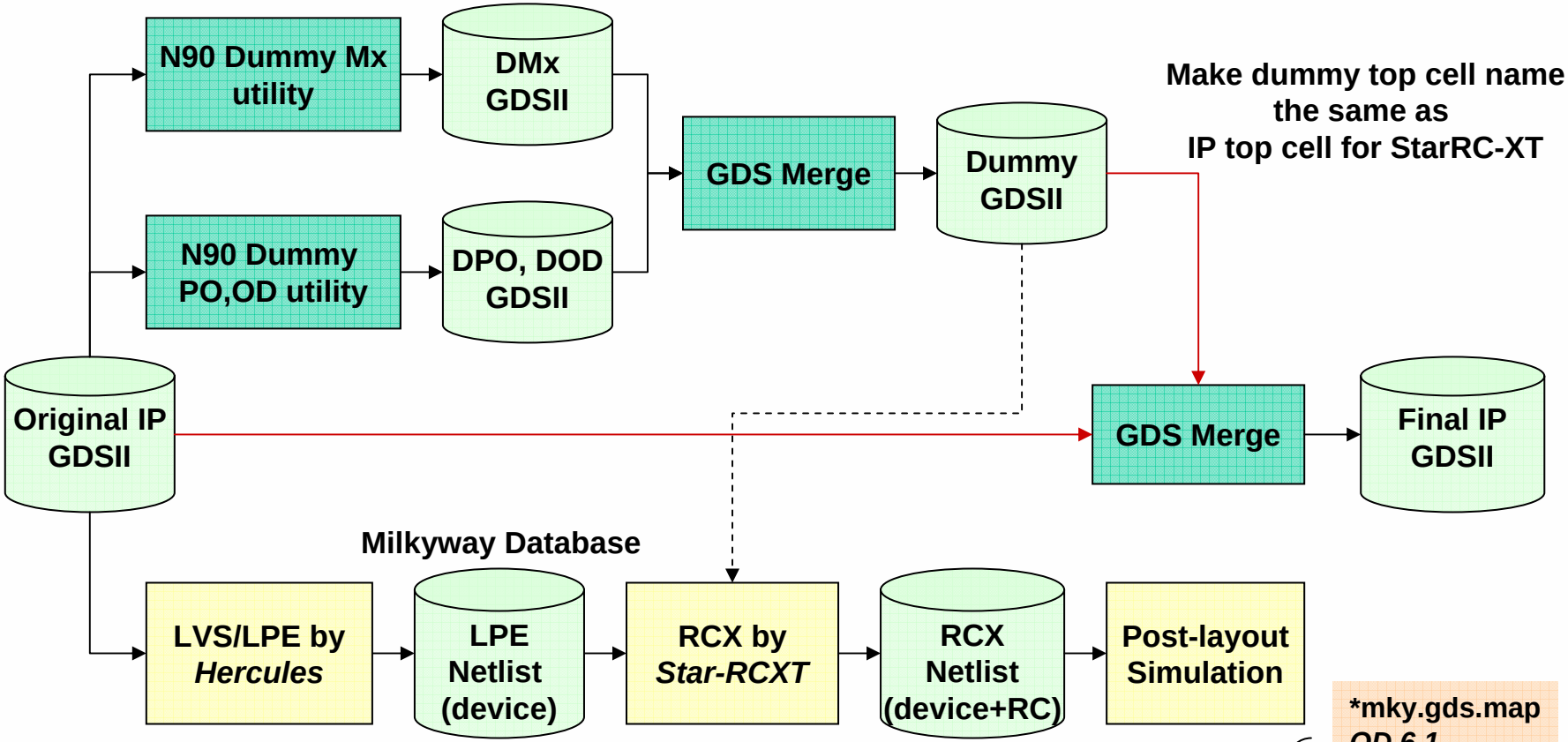
Dummy filling flow & Timing Fixing



Dummy Fill Guidelines

- In a cell-based design area, it's recommended to use filler cell with DPO/DOD for empty area (please refer TSMC N90 standard cell library).
- It's recommended to use TSMC fill utility for macro block and chip top level for final GDSII to guarantee global uniformity.
- If using TSMC fill utility for DM and DOD, low densities violations could be waived by TSMC PE. Otherwise, all densities rules should be met.
- Do dummy fill in a bottom-up approach.
  - Macro block meet rules and timing first, then chip level.

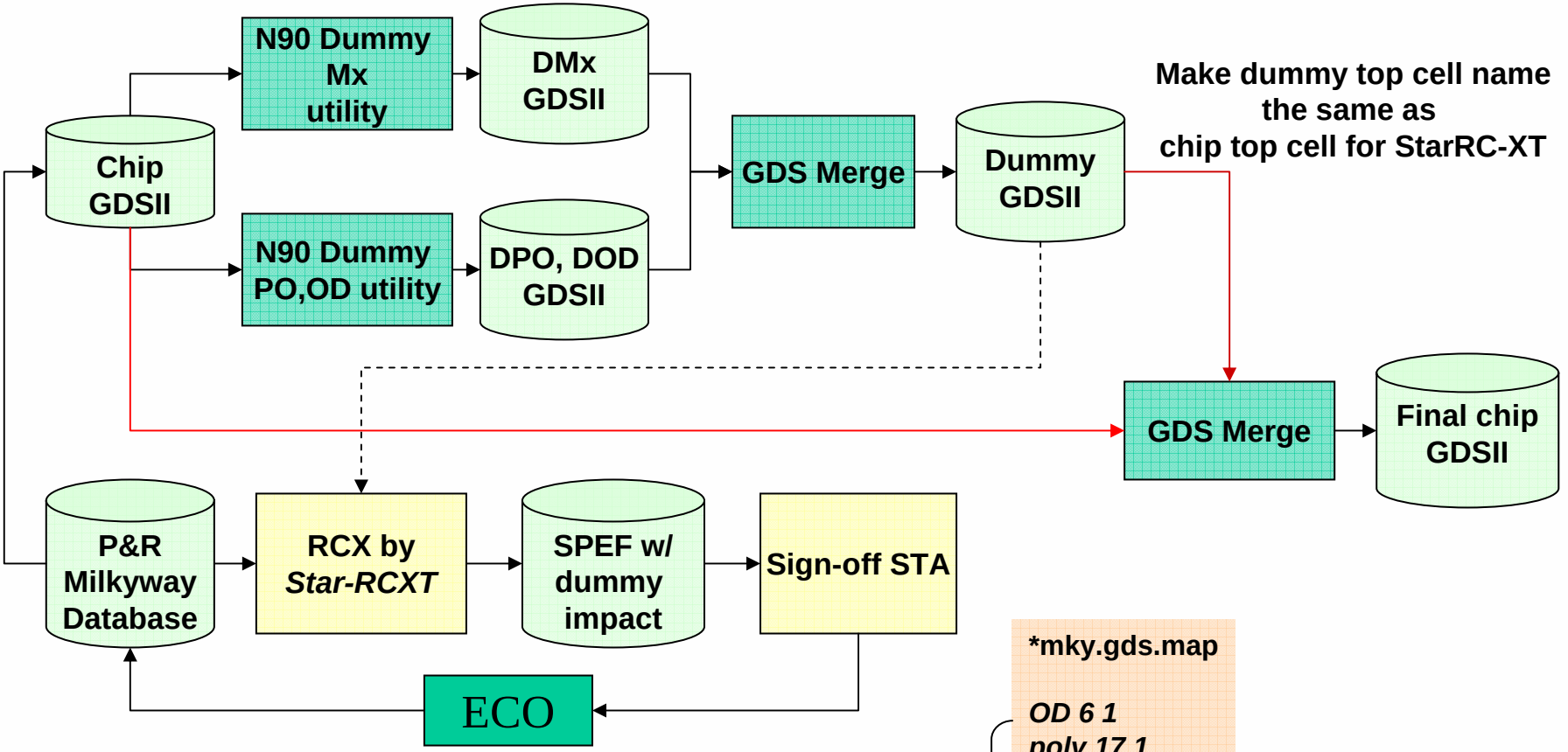
Macro IP Dummy Fill Timing Flow



*** Star-RCXT command file**
METAL_FILL_GDS_FILE: dummy.gds
GDS_LAYER_MAP_FILE: mky.gds.map
METAL_FILL_POLYGON_HANDLING: FLOAT

***mky.gds.map**
OD 6 1
poly 17 1
metal1 31 1
metal2 32 1
…
metal1 31 7
metal2 32 7
…

Top (Digital) Dummy Fill Timing Flow



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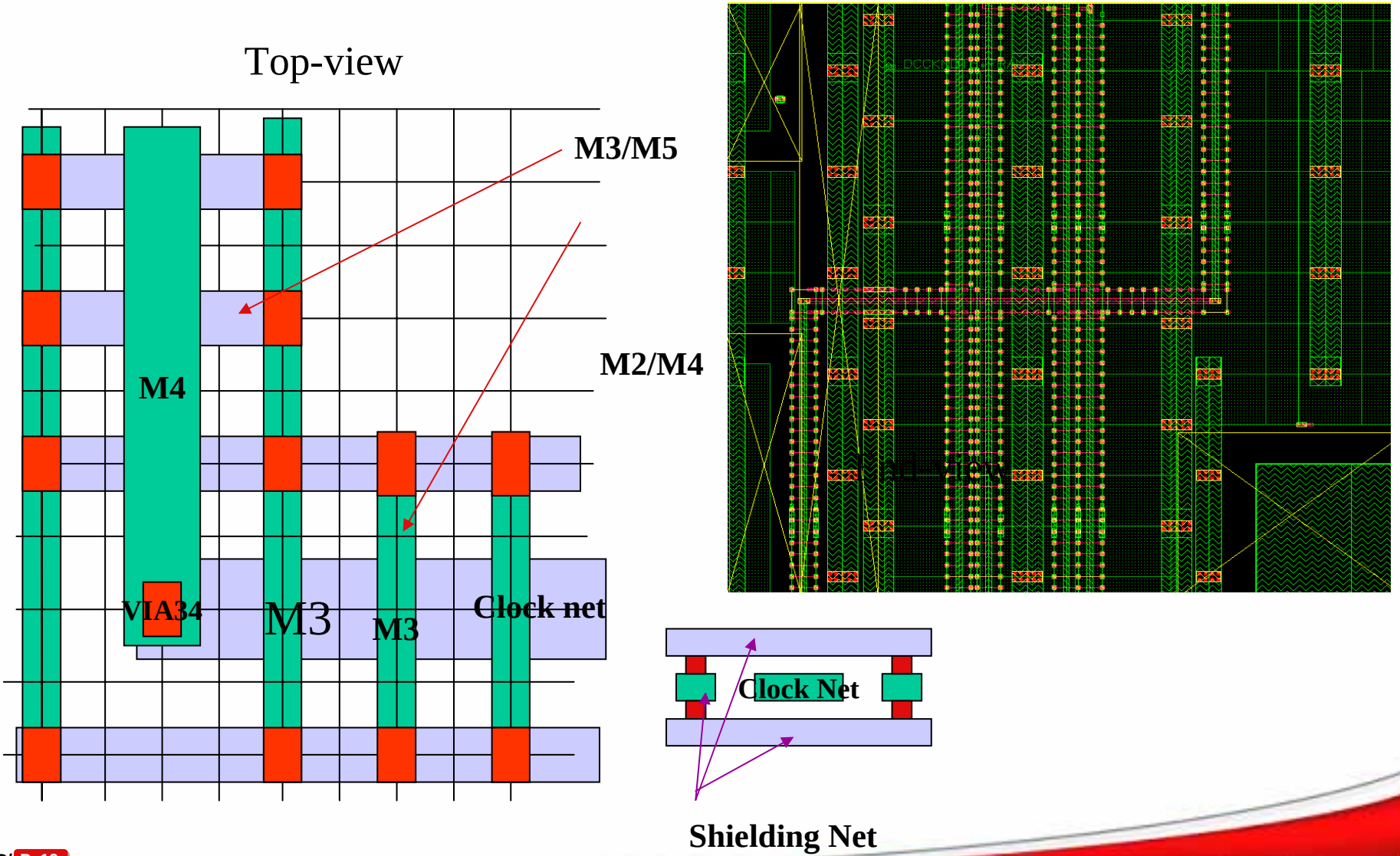
METAL_FILL_GDS_FILE: dummy.gds
GDS_LAYER_MAP_FILE: mky.gds.map
METAL_FILL_POLYGON_HANDLING: FLOAT

***mky.gds.map**

OD 6 1
poly 17 1
metal1 31 1
metal2 32 1
…
metal1 31 7
metal2 32 7
…

Others: High-Speed Clocks



Signoff Task vs. EDA Tool

	Task	EDA Tool	Major Role
Design tool	ATPG	Tmax/fastscan	Vector generation/simulation
	Floor plan	Astro/SOC encounter	Floor plan environment
	Placement/CTS/Route	Astro/SOC encounter	Placement/CTS/Route tool
	SI	Celtic	Xtalk analysis
	RC extraction	StarRC	RC extraction
Signoff	Netlist Handoff	Spyglass & Prime Time	Sanity Check
	LEC (Verplex)	LEC	formal validation
	Static IR	Voltage Storm	Static IR drop analysis
	Dynamic IR	RedHawk	Dynamic IR drop analysis
	Power EM	Voltage Storm	Power Ring reliability issue
	Signal EM	Astro/CISD utility	Signal wire reliability issue
	STA w/ Incr. SDF	Prime Time	Static timing analysis
	Redundant via insertion	Calibre/Laker/Virtuoso	Yield improvement
	Dummy metal insertion	Calibre/Laker/Virtuoso	Yield improvement
	Antenna	Calibre/Hermcules	Antenna effect check
	DRC/LVS/ERC	Calibre/Hercules	TSMC design rule checks